Features

- Typical 1.4 µA Ultra-low Quiescent Current
- Input Voltage Range: 2.4 V to 7 V
- Output Voltage Options:
  - Fixed: 1 V, 1.2 V, 1.8 V, 2.5 V, 2.8 V, 3 V, 3.3 V, 3.6 V
- ±1% Output Voltage Accuracy under Room Temperature
- Maximum Output Current: 200 mA
- Low Shutdown Current
- Low Dropout Voltage: 170 mV at 200 mA
- Current Limit and Thermal Protection
- Stable with 2.2 µF Ceramic Capacitor
- Active Output Discharge While Disable
- Soft-start Limits Input Current Surge During Enable
- Operating Temperature Range: −40°C to +85°C
- Packages: SOT23-3, SOT23-5, SOT89-3, 1×1 DFN-4

Applications

- Handheld Devices with Battery Power Supply
- Portable Devices with Battery Power Supply
- Wearable Application, Bluetooth Headsets
- Wireless and IoT modules
- Personal Electronics, Personal Healthcare

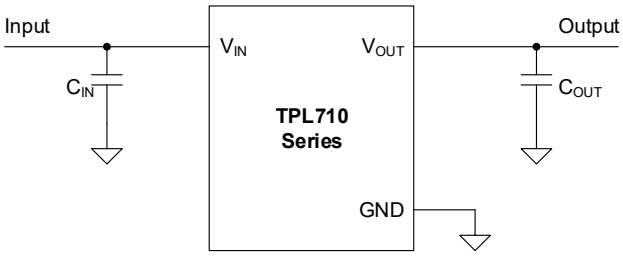
Description

The TPL710 series products are CMOS process low Iq linear regulators with enable control function. The TPL710 series products support maximum 200mA output current, with typically only 1.4 µA ultra-low quiescent current. TPL710 series products are stable with low-ESR small ceramic output capacitors from 2.2 µF to 10 µF.

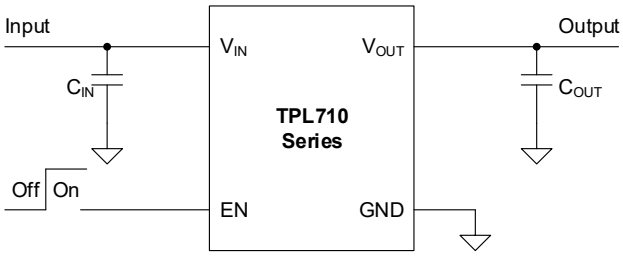
The TPL710 series products have fast response performance when load dynamic drop or raise, especially for the load dynamic from with some load. The TPL710 series products have current limit and thermal protection, which improves TPL710 series products with high reliability.

The TPL710 series products have a fixed output voltage range from 1 V to 3.6 V with ±1% output voltage accuracy, line regulation and load regulation under room temperature. The TPL710 series products are guaranteed over the operating temperature range of −40°C to +85°C. The TPL710 series products are available in SOT23-3 package, SOT23-5 package, SOT89-3 package, and 1×1 DFN-4 package.

Typical Application Schematic



TPL710 Series without Enable Pin



TPL710 Series with Enable Pin

Product Family Table

Part Number	Output Voltage	Order Number	Package	Transport Media, Quantity	MSL	Marking Information
TPL710F10	Fixed 1.0 V	TPL710F10-3TR	SOT23-3	Tape and Reel, 3,000	L3	L3C
TPL710F12	Fixed 1.2 V	TPL710F12-3TR	SOT23-3	Tape and Reel, 3,000	L3	L3D
TPL710F18	Fixed 1.8 V	TPL710F18-3TR	SOT23-3	Tape and Reel, 3,000	L3	L3F
TPL710F25	Fixed 2.5 V	TPL710F25-3TR	SOT23-3	Tape and Reel, 3,000	L3	L3G
TPL710F28	Fixed 2.8 V	TPL710F28-3TR	SOT23-3	Tape and Reel, 3,000	L3	L3H
TPL710F30	Fixed 3.0 V	TPL710F30-3TR	SOT23-3	Tape and Reel, 3,000	L3	L3I
TPL710F33	Fixed 3.3 V	TPL710F33-3TR	SOT23-3	Tape and Reel, 3,000	L3	L3J
TPL710F36	Fixed 3.6 V	TPL710F36-3TR	SOT23-3	Tape and Reel, 3,000	L3	L3K
TPL710F10	Fixed 1.0 V	TPL710F10-5TR	SOT23-5	Tape and Reel, 3,000	L3	L3C
TPL710F12	Fixed 1.2 V	TPL710F12-5TR	SOT23-5	Tape and Reel, 3,000	L3	L3D
TPL710F18	Fixed 1.8 V	TPL710F18-5TR	SOT23-5	Tape and Reel, 3,000	L3	L3F
TPL710F25	Fixed 2.5 V	TPL710F25-5TR	SOT23-5	Tape and Reel, 3,000	L3	L3G
TPL710F28	Fixed 2.8 V	TPL710F28-5TR	SOT23-5	Tape and Reel, 3,000	L3	L3H
TPL710F30	Fixed 3.0 V	TPL710F30-5TR	SOT23-5	Tape and Reel, 3,000	L3	L3I
TPL710F33	Fixed 3.3 V	TPL710F33-5TR	SOT23-5	Tape and Reel, 3,000	L3	L3J
TPL710F36	Fixed 3.6 V	TPL710F36-5TR	SOT23-5	Tape and Reel, 3,000	L3	L3K
TPL710F10	Fixed 1.0 V	TPL710F10-89TR	SOT89-3	Tape and Reel, 4,000	L3	L3C
TPL710F12	Fixed 1.2 V	TPL710F12-89TR	SOT89-3	Tape and Reel, 4,000	L3	L3D
TPL710F18	Fixed 1.8 V	TPL710F18-89TR	SOT89-3	Tape and Reel, 4,000	L3	L3F
TPL710F25	Fixed 2.5 V	TPL710F25-89TR	SOT89-3	Tape and Reel, 4,000	L3	L3G
TPL710F28	Fixed 2.8 V	TPL710F28-89TR	SOT89-3	Tape and Reel, 4,000	L3	L3H
TPL710F30	Fixed 3.0 V	TPL710F30-89TR	SOT89-3	Tape and Reel, 4,000	L3	L3I
TPL710F33	Fixed 3.3 V	TPL710F33-89TR	SOT89-3	Tape and Reel, 4,000	L3	L3J
TPL710F36	Fixed 3.6 V	TPL710F36-89TR	SOT89-3	Tape and Reel, 4,000	L3	L3K
TPL710F10	Fixed 1.0 V	TPL710F10-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L3C
TPL710F12	Fixed 1.2 V	TPL710F12-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L3D
TPL710F18	Fixed 1.8 V	TPL710F18-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L3F
TPL710F25	Fixed 2.5 V	TPL710F25-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L3G
TPL710F28	Fixed 2.8 V	TPL710F28-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L3H
TPL710F30	Fixed 3.0 V	TPL710F30-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L3I
TPL710F33	Fixed 3.3 V	TPL710F33-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L3J
TPL710F36	Fixed 3.6 V	TPL710F36-FR	1×1 DFN-4	Tape and Reel, 12,000	L3	L3K

Table of Contents

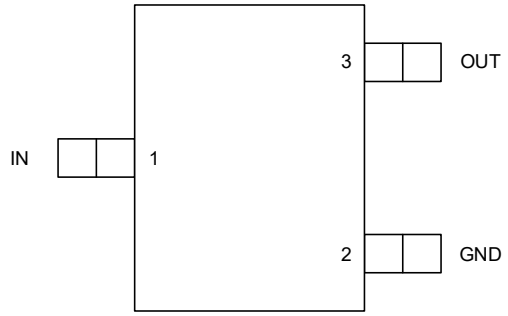
Revision History

Date	Revision	Notes
2018/09/08	Rev.Pre	Preliminary Version
2019/01/10	Rev.A.0	Initial Release
2019/08/30	Rev.A.1	1. Add 3.6V Output Voltage Option 2. Upgrade VIN Maximum Voltage to 7 V

Pin Configuration and Functions

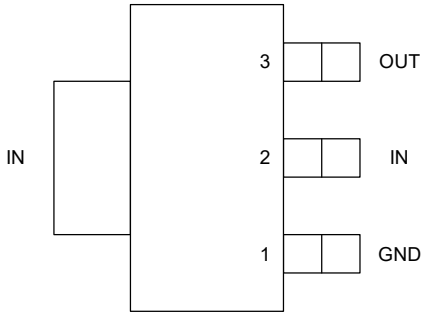
TPL710 Series

3-Pin SOT23 Package



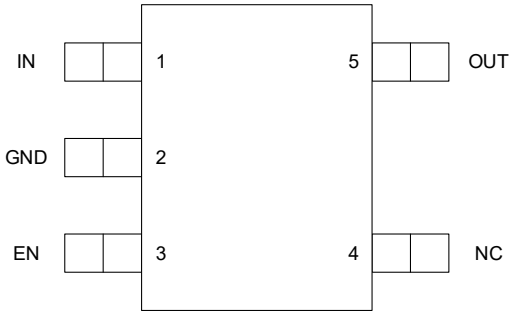
TPL710 Series

3-Pin SOT89 Package



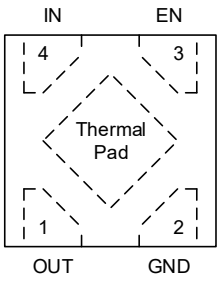
TPL710 Series

5-Pin SOT23 Package



TPL710 Series

4-Pin DFN Package



Pin Functions

Name	Pin Number				I/O	Description
	SOT23-3	SOT23-5	SOT89-3	DFN-4		
EN	–	3	–	3	I	Regulator enable pin. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to IN directly.
GND	2	2	1	2	–	Ground reference pin. Connect GND pin to PCB ground plane directly.
IN	1	1	2	4	I	Input voltage pin. Bypass IN to GND with a 1 µF or greater capacitor.
NC	–	4	–	–	–	No connection.
OUT	3	5	3	1	O	Regulated output voltage pin. Bypass OUT to GND with a 2.2 µF or greater capacitor.

Note: Thermal pad must be connected to PCB ground plane to maximum the thermal performance.

Specifications

Absolute Maximum Ratings

Parameters		Min	Max	Unit
V_{IN}, V_{EN}	Input Voltage	−0.3	7.5	V
V_{OUT}	Output Voltage	−0.3	7.5	V
T_J	Junction Temperature Range	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_L	Lead Temperature (Soldering 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) All voltage values are with respect to GND.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	±4	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	±1	kV

Recommended Operating Conditions

Parameters		Min	Max	Unit
V_{IN}	Input Voltage	2.4	7	V
V_{EN}	Enable Voltage	0	V_{IN}	V
V_{OUT}	Output Voltage	0	5	V
I_{OUT}	Output Current	0	200	mA
T_J	Operating Junction Temperature Range	−40	125	°C
T_A	Operating Ambient Temperature Range	−40	85	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
SOT23-3	280	62	°C/W
SOT23-5	280	62	°C/W
SOT89-3	55	88	°C/W
1×1 DFN-4	210	110	°C/W

Electrical Characteristics

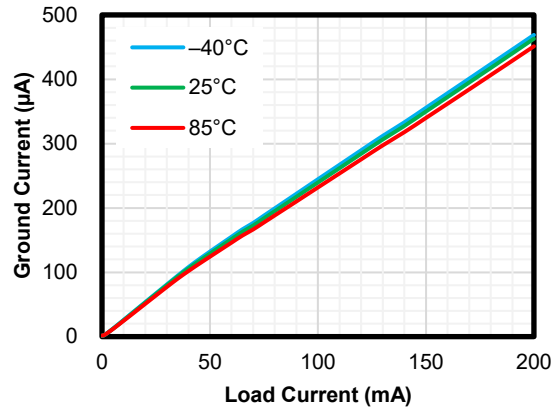
All test condition: V_{IN} = $V_{OUT(NOM)}$ + 1 V or 2.4 V, whichever is greater; C_{OUT} = 2.2 μF, T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Input Voltage and Current						
V_{IN}	Input voltage range		2.4		7	V
I_{GND}	Ground pin current	I_{OUT} = 0 mA		1.4		μA
		V_{IN} = 5 V, I_{OUT} = 200 mA		500		μA
I_{SHDN}	Shutdown current	EN = GND (4-/5-Pin Package Only)		0.1		μA
UVLO	V_{IN} under-voltage lock-out	V_{IN} rising		1.8		V
		Hysteresis		200		mV
Enable Input Voltage and Current (4-/5-Pin Package Only)						
$V_{IH(EN)}$	EN logic-input high level (enable)		1.2		V_{IN}	V
$V_{IL(EN)}$	EN logic-input low level (disable)		0		0.4	V
I_{EN}	EN pin leakage current	EN = V_{IN}		20		nA
Regulated Output Voltage and Current						
V_{OUT}	Output voltage accuracy	I_{OUT} = 30 mA, T_J = +25°C		1%		
		I_{OUT} = 30 mA, –40°C ≤ T_J ≤ +125°C	−3%		3%	
ΔV_{OUT}	Line regulation	V_{IN} = $V_{OUT(NOM)}$ + 1 V to 6 V, or V_{IN} ≥2.4V, I_{OUT} = 1 mA		3		mV
	Load regulation	I_{OUT} = 1 mA to 200 mA		40		mV
V_{DO} (1)	Dropout voltage	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 50 mA		40		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 100 mA		80		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 200 mA		170		mV
I_{OUT}	Output current	V_{OUT} in regulation	0		200	mA
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	300	560	800	mA
R_{DIS}	Output discharge resistance	V_{IN} = $V_{OUT(NOM)}$ + 1 V, EN = GND		190		Ω
PSRR	Power supply rejection ratio	I_{OUT} = 10 mA, f = 100 Hz, C_{OUT} = 2.2 μF		55		dB
		I_{OUT} = 10 mA, f = 1 kHz, C_{OUT} = 2.2 μF		54		dB
		I_{OUT} = 10 mA, f = 10 kHz, C_{OUT} = 2.2 μF		50		dB
		I_{OUT} = 10 mA, f = 1 MHz, C_{OUT} = 2.2 μF		53		dB
V_N	Output noise voltage	I_{OUT} = 10 mA, BW = 10Hz to 100 kHz		90		μV_{RMS}
t_{STR}	Start-up time from EN assertion to 0.98 × $V_{OUT(NOM)}$	I_{OUT} = 200 mA, C_{OUT} = 2.2 μF		680		μs
Temperature Range						
T_{SD}	Thermal shutdown temperature			165		ºC
	Thermal shutdown hysteresis			15		ºC

***Note:** (1). Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to: V_{IN} – $V_{DROPOUT}$.

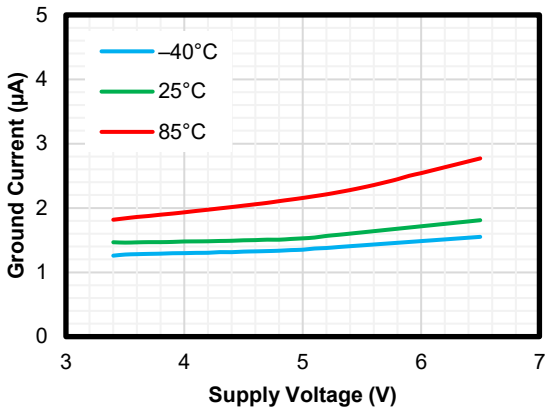
Typical Performance Characteristics

All test condition: V_{IN} = $V_{OUT(NOM)}$ + 1 V or 2.4 V, whichever is greater; C_{OUT} = 2.2 µF, T_A = +25°C, unless otherwise noted.



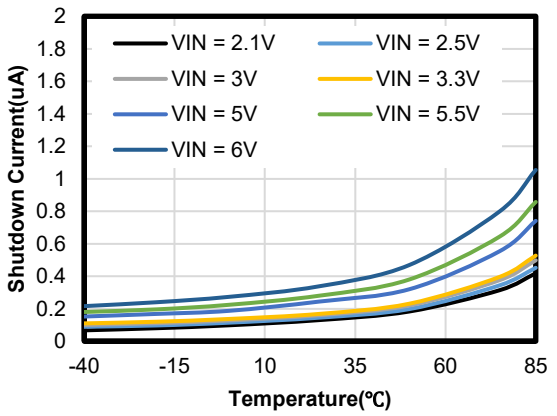
V_{OUT} = 3.3V

Figure 1 Ground Current vs Output Current



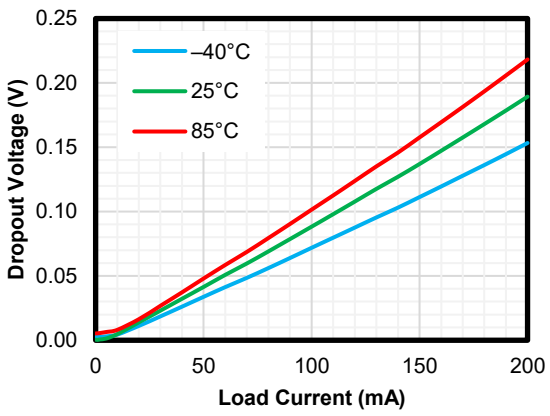
V_{OUT} = 3.3V

Figure 2 Quiescent Current vs Input Voltage



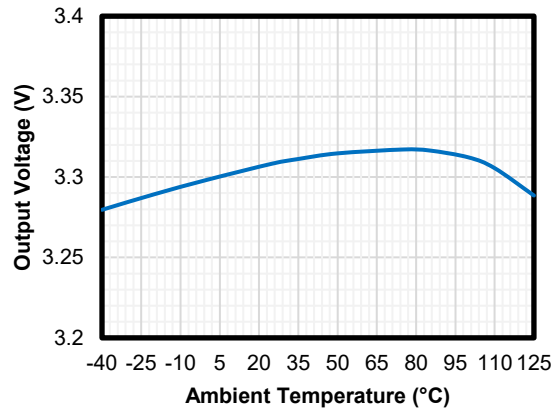
With Enable Pin

Figure 3 Shutdown Current vs Ambient Temperature



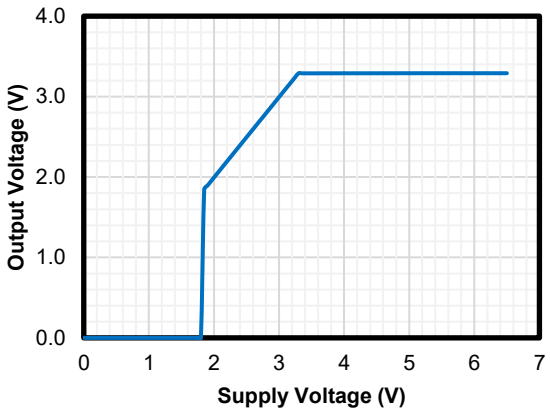
V_{OUT} = 3.3V

Figure 4 Dropout Voltage vs Output Current



V_{OUT} = 3.3V

Figure 5 Output Accuracy vs Ambient Temperature

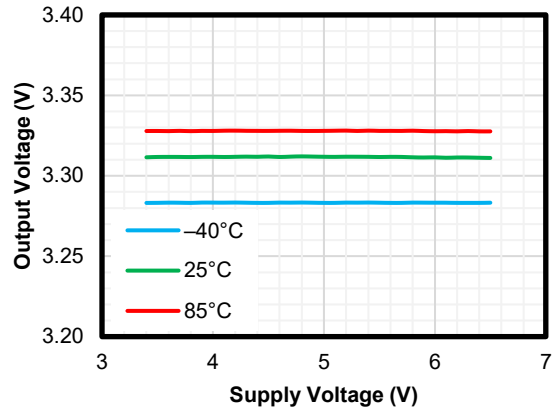


V_{OUT} = 3.3V

Figure 6 Output Voltage vs Input Voltage

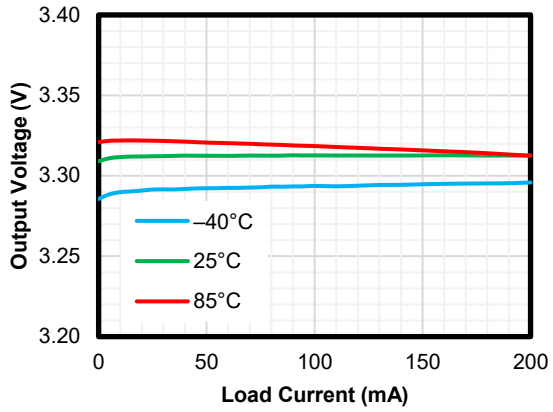
Typical Performance Characteristics (continued)

Test condition: V_{IN} = $V_{OUT(NOM)}$ + 1 V or 2.4 V, whichever is greater; C_{OUT} = 2.2 µF, T_A = +25°C, unless otherwise noted.



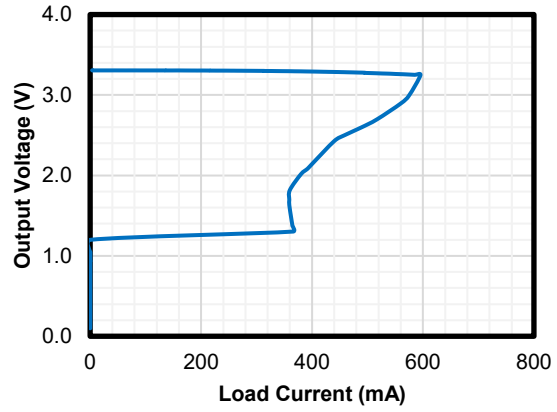
V_{OUT} = 3.3V

Figure 7. Line Regulation



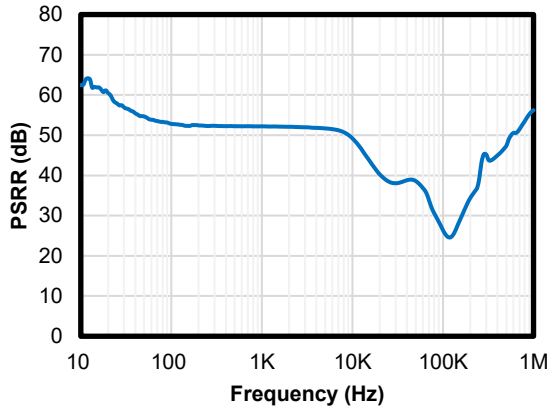
V_{OUT} = 3.3V

Figure 8. Load Regulation



V_{OUT} = 3.3V

Figure 9. Current Limit



V_{OUT} = 3.3V I_{OUT} = 10 mA C_{OUT} = 2.2 µF

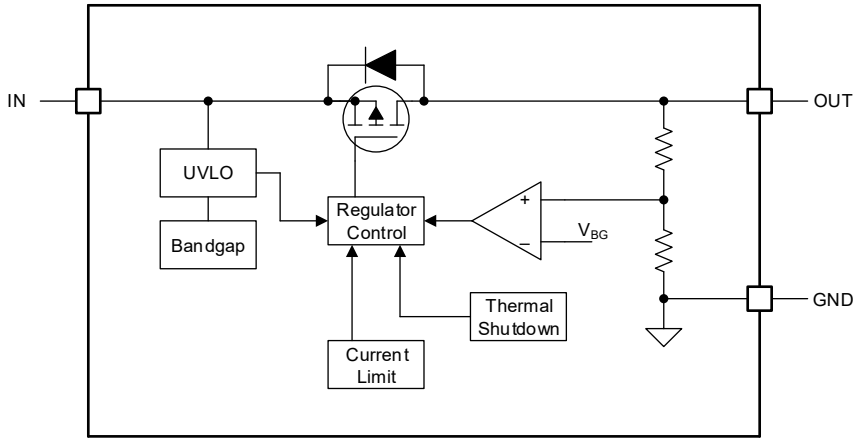
Figure 10. PSRR

Detailed Description

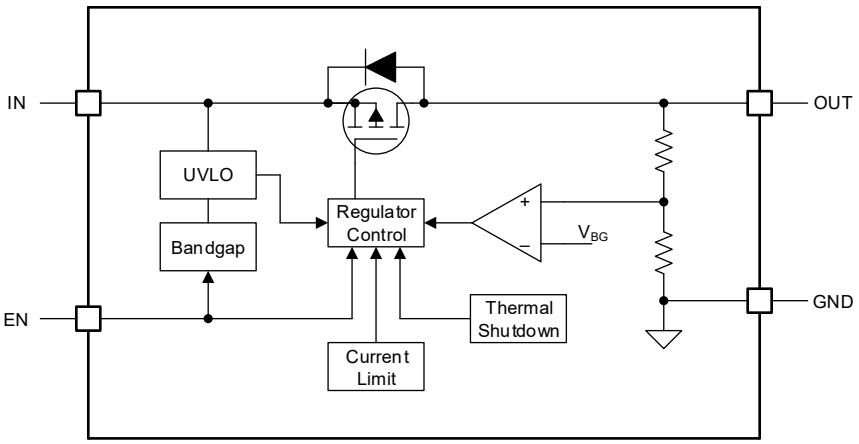
Overview

The TPL710 series products are CMOS process low Iq linear regulators with ultra-low quiescent power consumption. The TPL710 series products support maximum 200mA output current, with typically only 1.4 µA quiescent current. TPL710 series products are stable with low-ESR small ceramic output capacitor from 2.2 µF to 10 µF. The TPL710 series products are available in fixed voltage versions of 1V, 1.2 V, 1.8 V, 2.5 V, 2.8 V, 3 V, 3.3 V and 3.6 V.

Functional Block Diagram



TPL710 Series without Enable Pin



TPL710 Series with Enable Pin

Feature Description

Enable (4-/5-Pin Package Only)

The enable pin (EN) is active high. Connect this pin to the GPIO of an external processor or digital logic control circuit to enable and disable the device. Or connect this pin to the IN pin for self-bias applications.

Under-voltage Lockout (UVLO)

The TPL710 series use an under-voltage lockout circuit (UVLO = 1.8 V) to keep the output shut off until the internal circuitry operates properly.

Regulated Output Voltage

The TPL710 series are available in fixed voltage versions of 1V, 1.2 V, 1.8 V, 2.5 V, 2.8 V, 3 V, 3.3 V and 3.6 V. When the input voltage is higher than $V_{OUT(NOM)}$ + V_{DO} or 2.4V, output pin is the regulated output based on the selected voltage version. When the input voltage falls below $V_{OUT(NOM)}$ + V_{DO} or 2.4V, output pin tracks the input voltage minus the dropout voltage based on the load current. When the input voltage drops below UVLO threshold, the output keeps shut off.

Current Limit

The TPL710 series integrate an internal current limit that helps to protect the regulator during fault conditions. When the output is overloaded or shorted to ground, the LDO supplies output current with limited value to prevent the regulator from damage. Output voltage is not regulated when the device is in current limit mode, and the value is $V_{OUT} = I_{CL} \times R_{LOAD}$.

Thermal Shutdown

During normal operation, LDO junction temperature should not exceed 125°C. When the junction temperature exceeds the thermal shutdown threshold, the LDO shut down the output immediately. Until when the junction temperature falls below the thermal shutdown threshold minus thermal shutdown hysteresis, the output turns on again.

Application and Implementation

NOTE

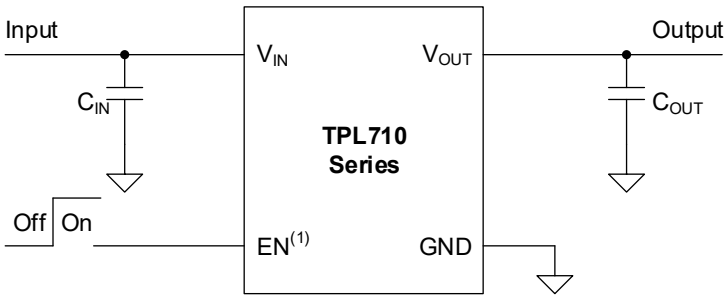
Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPL710 devices are a series of 200 mA high PSRR, low-dropout linear regulator with low quiescent current. The following application schematic shows a typical usage of the TPL710 series.

Typical Application

Figure 11 shows the typical application schematic of the TPL710 series.



(1) EN pin is only available in 4-/5-pin package

Figure 11 TPL710 Series Application Schematic

Input Capacitor and Output Capacitor

3PEAK recommends adding a 1 µF or greater capacitor with a 0.1 µF bypass capacitor in parallel at IN pin to keep the input voltage stable. The voltage rating of the capacitors must be greater than the maximum input voltage.

To ensure loop stability, the TPL710 series requires an output capacitor with a minimum effective capacitance value of 1 µF. 3PEAK recommends selecting a X5R- or X7R-type 2.2 µF or larger ceramic capacitor with low ESR over temperature.

Both input capacitors and output capacitors must be placed as close to the device pins as possible.

Power Dissipation

During normal operation, LDO junction temperature should not exceed 125°C. Using below equations to calculate the power dissipation and estimate the junction temperature.

The power dissipation can be calculated using Equation 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad (1)$$

The junction temperature can be estimated using Equation 2. θ_{JA} is the junction-to-ambient thermal resistance (See Section *Thermal Information*).

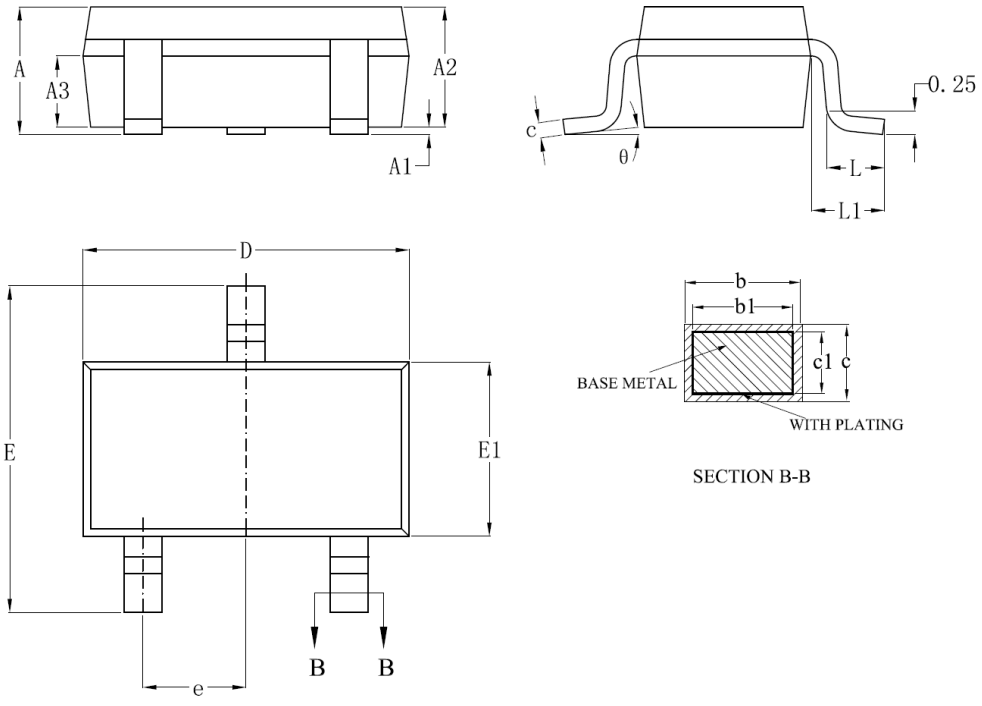
$$T_J = T_A + P_D \times \theta_{JA} \quad (2)$$

Layout Requirements

- Both input capacitors and output capacitors must be placed as close to the device pins as possible.
- It is recommended to bypass the input pin to ground with a 0.1 μF bypass capacitor. The loop area formed by the bypass capacitor connection, IN pin and the GND pin of the system must be as small as possible.
- It is recommended to use wide trace lengths or thick copper weight to minimize I×R drop and heat dissipation.

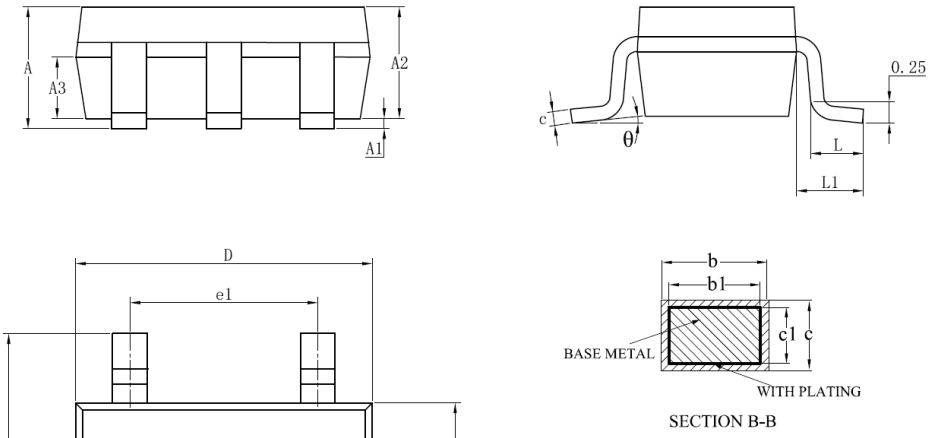
Package Outline Dimensions

SOT23-3



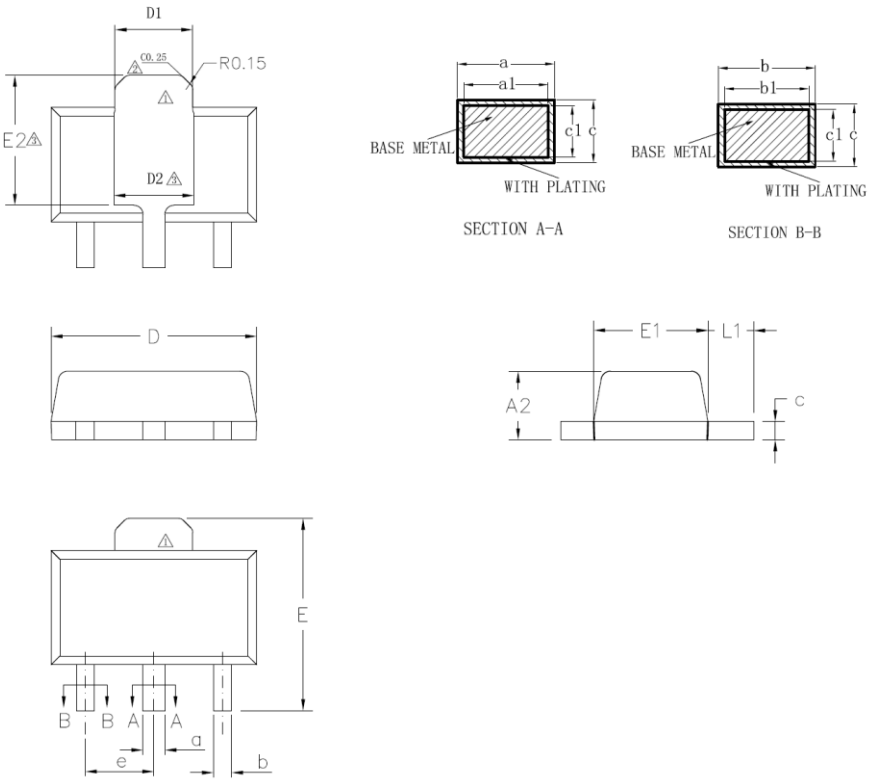
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.25
A1	0.04	—	0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95BSC		
L	0.30	—	0.60
L1	0.60REF		
θ	0	—	8°

SOT23-5



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.25
A1	0.04	—	0.10
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.33	—	0.41
b1	0.32	0.35	0.38
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95BSC		
e1	1.90BSC		
L	0.30	—	0.60
L1	0.60REF		
θ	0	—	8°

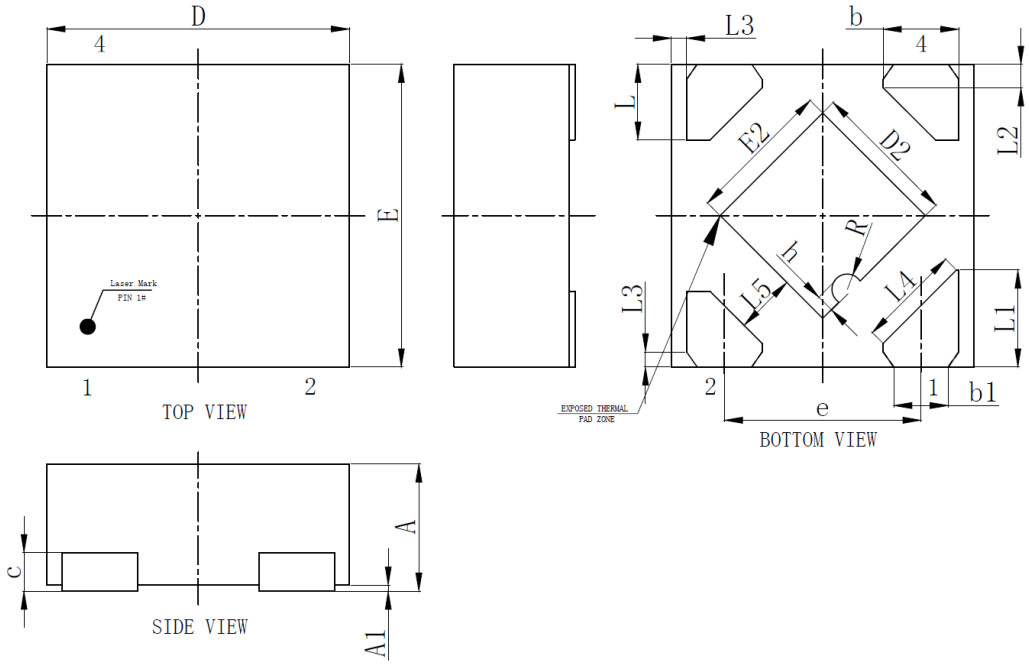
SOT89-3



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A2	1.40	1.50	1.60
b	0.38	—	0.46
b1	0.37	0.40	0.43
c	0.38	—	0.42
c1	0.37	0.38	0.39
a	0.46	—	0.56
a1	0.45	0.48	0.51
D	4.40	4.50	4.60
D1	1.62	—	1.83
E	3.95	—	4.25
E1	2.40	2.50	2.60
e	1.50BSC		
L1	0.89	—	1.20

L/F Size (mil) \ Size(mm)	D2	E2
66.9*63	1.75REF	2.84REF

1×1 DFN-4



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
b1	0.13	0.18	0.23
c	0.07	0.12	0.17
D	0.95	1.00	1.05
D2	0.43	0.48	0.53
e	0.65BSC		
E	0.95	1.00	1.05
E2	0.43	0.48	0.53
L	0.20	0.25	0.30
L1	0.27	0.32	0.37
L2	0.077REF		
L3	0.05REF		
L4	0.34REF		
L5	0.20REF		
R	0.05REF		
h	0.06REF		