DIO6805/6806
Ultra Low Power Microprocessor Reset Circuit

Features

- 13ms min Reset Pulse Width
- 10μA Supply Current @V_{CC}=3V
- Guaranteed Reset Valid to V_{CC}=1.0V
- Temperature coefficient of reset threshold: 21ppm/°C
- Power Supply Transient Immunity
- Operating Temperature Range：-40°C to 125°C
- Available in SOT23

Applications

- Computers
- Controllers
- Intelligent Instruments
- Portable/Battery-Powered Equipment

Descriptions

DIO6805/6806 series are micro-processor (μP) supervisory circuits used to monitor the power supplies in μP and digital systems. They provide excellent circuit reliability and low cost by eliminating external components.

These circuits perform a single function: they assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 13ms after V_{CC} has risen above the reset threshold.

The DIO6805/6806 has CMOS outputs. The DIO6805 has an active-low /RESET output, while the DIO6806 has an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}, and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 1.0V over the temperature range.

The device is available in 3pin SOT23 package.

Ordering Information

Order Part Number		T_A	Package	
DIO6805XST3	RoHS	-40 to 125°C	SOT23	Tape & Reel, 3000
DIO6806XST3	RoHS	-40 to 125°C	SOT23	Tape & Reel, 3000

Ordering Information Complimentary Note

Ordering Code = Part No. + Package Code

ST3: stands for SOT23

X: Refer to Device Function Reference Table on Page 2

Device Function Reference Table

Part No.	Reset threshold	Reset active Low or High	Output Type	Marking
DIO6805L	4.63V	Low	CMOS	ANAA
DIO6806L	4.63V	High	CMOS	BNAA
DIO6805M	4.38V	Low	CMOS	APAA
DIO6806M	4.38V	High	CMOS	BPAA
DIO6805J	4.00V	Low	CMOS	CUAA
DIO6806J	4.00V	High	CMOS	DUAA
DIO6805T	3.08V	Low	CMOS	AQAA
DIO6806T	3.08V	High	CMOS	BQAA
DIO6805S	2.93V	Low	CMOS	ARAA
DIO6806S	2.93V	High	CMOS	BRAA
DIO6805R	2.63V	Low	CMOS	ASAA
DIO6806R	2.63V	High	CMOS	BSAA
DIO6805Z	2.32V	Low	CMOS	ATAA
DIO6806Z	2.32V	High	CMOS	BTAA

Pin Assignment

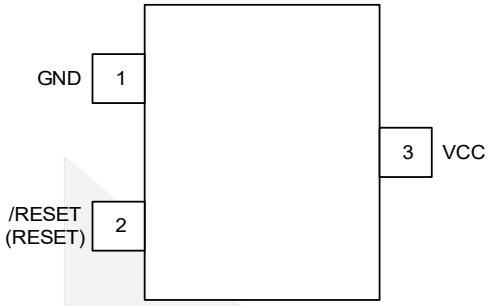


Figure 1 Pin Assignment (Top View)

Pin Descriptions

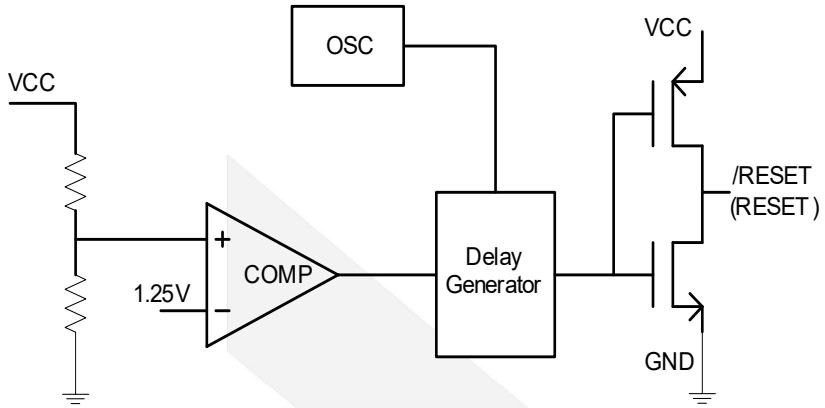
Symbol	Description
GND	Ground terminal.
/RESET (DIO6805)	CMOS output. This output remains low if V_{CC} drops below V_{RES}, and for at least 13ms after V_{CC} rises above $V_{RES}+V_{HYST}$.
RESET (DIO6806)	CMOS output. This output remains high if V_{CC} drops below V_{RES}, and for at least 13ms after V_{CC} rises above $V_{RES}+V_{HYST}$.
VCC	Analog input. This pin is both the power supply to internal circuit and the voltage to be monitored.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter		Rating	Units
Terminal Voltage (With respect to GND)	V_{CC}	-0.3 to 6.0	V
	/RESET, RESET	-0.3 to 6.0	
Input Current	V_{CC}	20	mA
	/RESET, RESET	20	
Thermal Resistance		300	°C/W
Operating Temperature		-40 to 125	°C
Lead Temperature Range (soldering 10s)		300	°C
Storage Temperature		-65 to 150	°C
ESD HBM, JEDEC: JESD22-A114		4500	V

Block Diagram



DC Electrical Characteristics

Typical value: V_{CC}=3V, T_A=25°C, unless otherwise noted.

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum input voltage	V_{CCMAX}				5.5	V
Minimum input voltage	V_{CCMIN}		1.0			V
Supply current	I_{VCC}	Vcc=2.0V		8		uA
		Vcc=3.0V		10		
		Vcc=5.0V		14		
Reset Threshold	V_{RES}	DIO68_L	4.51	4.63	4.75	V
		DIO68_M	4.25	4.38	4.5	
		DIO68_J	3.9	4.00	4.1	
		DIO68_T	3.0	3.08	3.15	
		DIO68_S	2.85	2.93	3.00	
		DIO68_R	2.56	2.63	2.7	
		DIO68_Z	2.26	2.32	2.38	
Temperature coefficient of reset threshold	T_C			21		ppm/°C
Reset Threshold hysteresis	V_{HYST}			0.03V_{RES}		V
V_{CC} to /RESET Delay (DIO6805)		V_{CC} transitions from V_{RES}+0.1V to V_{RES}-0.1V		23		us
V_{CC} to RESET Delay (DIO6806)		V_{CC} transitions from V_{RES}+0.1V to V_{RES}-0.1V		23		us

/RESET Output Voltage Low (DIO6805)	V_{OL}	V_{CC}=2V, V_{RES}>2V, I_{SINK}=1.5mA			0.3	V
		V_{CC}=3V, V_{RES}>3V, I_{SINK}=3.2mA			0.3	
		V_{CC}=4V, V_{RES}>4V, I_{SINK}=5mA			0.3	
/RESET Output Voltage High (DIO6805)	V_{OH}	V_{CC}=3V, V_{RES}<3V, I_{SOURCE}=1.2mA	V_{CC}-0.4			V
		V_{CC}=4V, V_{RES}<4V, I_{SOURCE}=2mA	V_{CC}-0.4			
		V_{CC}=5V, V_{RES}<5V, I_{SOURCE}=2.5mA	V_{CC}-0.4			
RESET Output Voltage Low (DIO6806)	V_{OL}	V_{CC}=3V, V_{RES}<3V, I_{SINK}=3.2mA			0.3	V
		V_{CC}=4V, V_{RES}<4V, I_{SINK}=5mA			0.3	
		V_{CC}=5V, V_{RES}<5V, I_{SINK}=6mA			0.3	
RESET Output Voltage High (DIO6806)	V_{OH}	V_{CC}=2V, V_{RES}>2V, I_{SOURCE}=600uA	V_{CC}-0.4			V
		V_{CC}=3V, V_{RES}>3V, I_{SOURCE}=1.2mA	V_{CC}-0.4			
		V_{CC}=4V, V_{RES}>4V, I_{SOURCE}=2mA	V_{CC}-0.4			
Reset Pulse Width	T_{RES}		13	25	50	ms

Specifications subject to change without notice.

Applications Information

A microprocessor's (μP's) reset input starts the μP in a known state. The DIO6805/6806 series assert reset to prevent code-execution errors during power-up, power-down, or brownout conditions. The device consists of a comparator, a low current high precision voltage reference, voltage divider, output delay circuit and output driver. They assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 13ms after V_{CC} has risen above the reset threshold.

The DIO6805/6806 have a CMOS output stage. The DIO6805 have an active-low /RESET output, while the DIO6806 have an active-high RESET output. The reset comparator is designed to ignore fast transients on V_{CC}, and the outputs are guaranteed to be in the correct logic state for V_{CC} down to 1.0V over the temperature range. The operation of the device can be best understood by referring to figure 2.

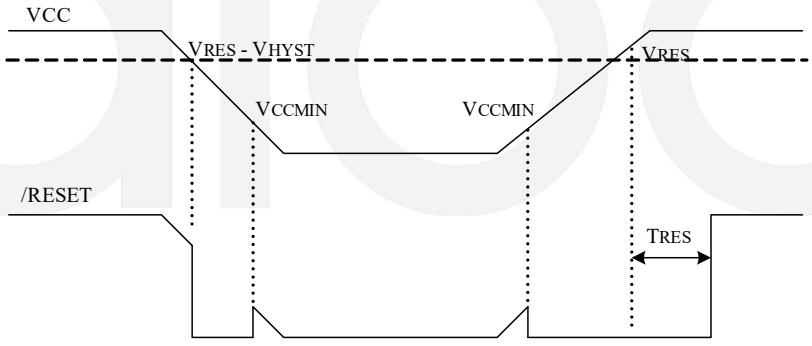


Figure 2

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the DIO6805/6806 series are relatively immune to short-duration negative-going V_{CC} transients (glitches). As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 10µs or less will not cause a reset pulse. A 0.1µF bypass capacitor mounted as close as possible to the V_{CC} pin provides additional transient immunity.

Ensuring a Valid Reset Output Down to V_{CC} = 0

When V_{CC} falls below 1.0V, the DIO6805 /RESET output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to /RESET can drift to undetermined voltages. This presents no problem in most applications, since most µP and other circuitry is inoperative with V_{CC} below 1.0V.

However, in applications where /RESET must be valid down to 0V, a pull-down resistor is needed from /RESET pin to GND as shown in Figure 3, then /RESET output will be held at low state. The resistor's value is not critical, it should be about 100KΩ, large enough not to load /RESET, small enough to pull /RESET to ground.

A 100KΩ pull-up resistor to V_{CC} is also recommended for the DIO6806 if active high RESET is required to remain valid for V_{CC} < 1.0V.

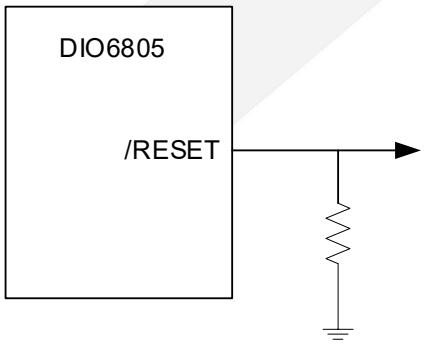
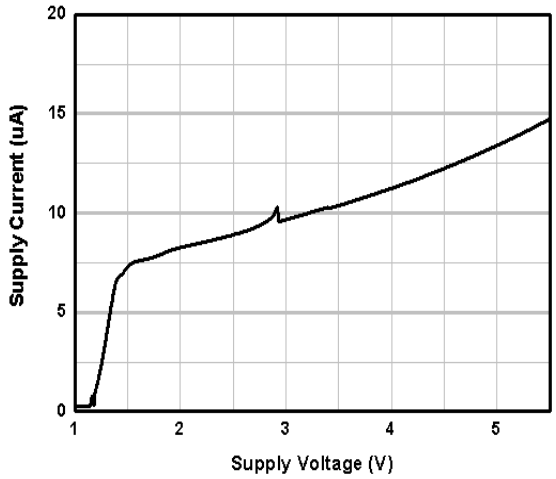


Figure 3 RESET Valid to Ground Circuit

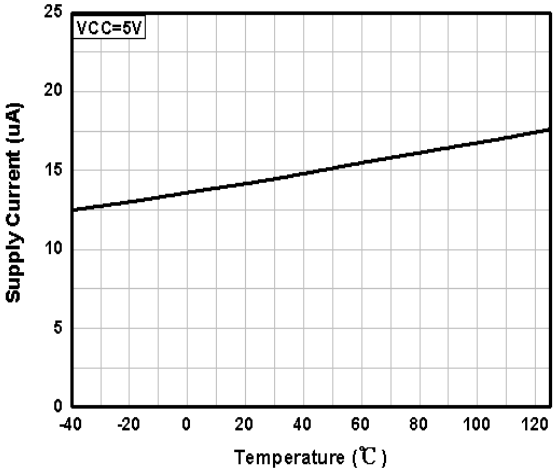
Typical Performance Characteristics

All typical value: V_{CC}=5V, T_A=25°C, unless otherwise specified.

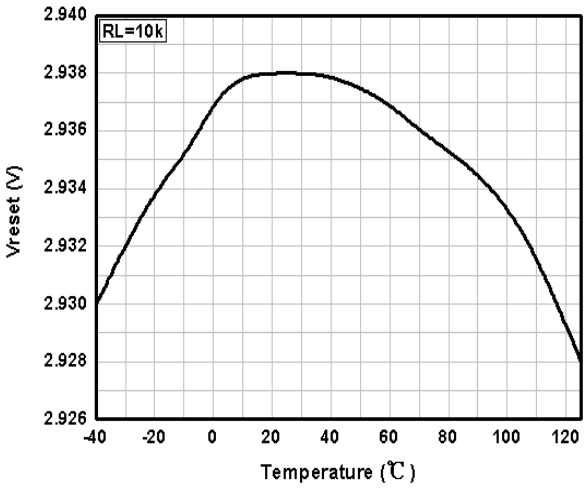
Supply Current vs.Supply Voltage



Supply Current vs.Temperature



Reset Threshold vs.Temperature



CONTACT US

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