DIO6811/6812
Ultra Low Power Microprocessor Reset Circuit

Features

- Specified over Temperature
- Low Power Consumption
- Precision Voltage Monitor: 2.5V, 3V, 3.3V, 5V Options
- Reset Assertion Down to 1V VCC
- 160ms Min Power-On Reset
- Temperature coefficient of reset threshold: 21ppm/°C
- Logic Low /RESET Output (DIO6811)
- Logic High RESET Output (DIO6812)
- Manual Reset Input
- Compact 4-Pin SOT143 and 5-Pin SOT23 Packages

Applications

- Microprocessor Systems
- Controllers
- Intelligent Instruments
- Automotive Systems
- Safety Systems
- Portable Instruments

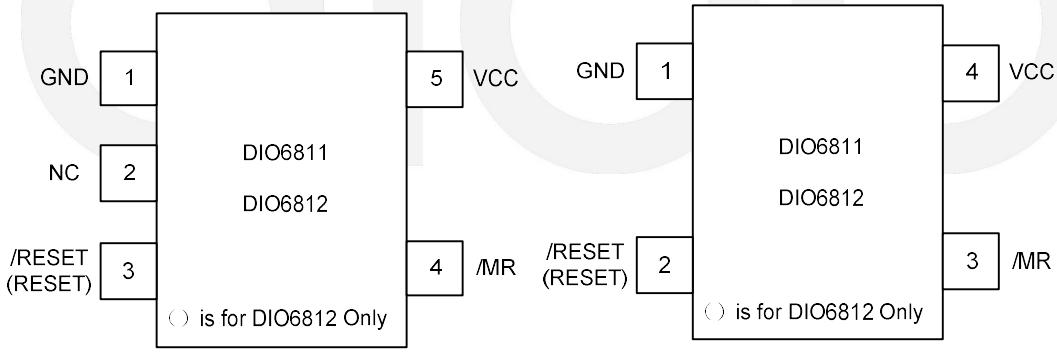
Descriptions

The DIO6811/6812 supervisory circuits monitor the power supply voltage in microprocessor and digital systems. The DIO6811/6812 is designed to monitor seven different voltages, these voltages have been selected for the effective monitoring of 2.5V, 3V, 3.3V, and 5V supply voltage levels.

They provide a reset output during power-up, power-down and brownout conditions. On power-up, an internal timer holds reset asserted for 240ms. This holds the microprocessor in a reset state until conditions have stabilized. The /RESET output remains operational with VCC as low as 1V. The DIO6811 provides an active low reset signal (/RESET) while the DIO6812 provides an active high signal (RESET) output.

The DIO6811/6812 has a manual reset input. The manual reset function is very useful, especially if the circuit in which the DIO6811/6812 is operating enters into a state that can only be detected by the user. Allowing the danger that could otherwise be caused by an out-of-control or locked system. The devices come in a 4-pin SOT143 and 5-pin SOT23 packages.

Pin Assignment



Ordering Information

Order Part Number		T_A	Package	
DIO6811XST5	RoHS	-40 to 125°C	SOT23-5	Tape & Reel, 3000
DIO6811XST4	RoHS	-40 to 125°C	SOT143-4	Tape & Reel, 3000
DIO6812XST5	RoHS	-40 to 125°C	SOT23-5	Tape & Reel, 3000
DIO6812XST4	RoHS	-40 to 125°C	SOT143-4	Tape & Reel, 3000

Ordering Information Complimentary Note

Ordering Code = Part No. + Package Code

ST5: stands for SOT23-5

ST4: stands for SOT143-4

X: Refer to Device Function Reference

Device Function Reference Table

Part No.	Reset threshold	Reset active Low or High	Output Type	Marking
DIO6811L	4.63V	Low	CMOS	W11L
DIO6812L	4.63V	High	CMOS	W12L
DIO6811M	4.38V	Low	CMOS	W11M
DIO6812M	4.38V	High	CMOS	W12M
DIO6811J	4.00V	Low	CMOS	W11J
DIO6812J	4.00V	High	CMOS	W12J
DIO6811T	3.08V	Low	CMOS	W11T
DIO6812T	3.08V	High	CMOS	W12T
DIO6811S	2.93V	Low	CMOS	W11S
DIO6812S	2.93V	High	CMOS	W12S
DIO6811R	2.63V	Low	CMOS	W11R
DIO6812R	2.63V	High	CMOS	W12R
DIO6811Z	2.32V	Low	CMOS	W11Z
DIO6812Z	2.32V	High	CMOS	W12Z

Pin Descriptions

Symbol	Description
GND	Ground terminal.
NC	No Connect.
/RESET (DIO6811)	Active Low Logic Output. /RESET remains low while VCC is below the reset threshold or when /MR is low; /RESET then remains low for at least 160ms after VCC rises above the reset threshold.
RESET (DIO6812)	Active High Logic Output. RESET remains high while VCC is below the reset threshold or when /MR is low; RESET then remains high for 240ms (typical) after VCC rises above the reset threshold.
/MR	Manual Reset. This active low debounced input will ignore input pulses of 100ns or less (typical) and is guaranteed to accept input pulses of greater than 10μs. Leave floating when not used.
V_{CC}	Analog input. This pin is both the power supply to internal circuit and the voltage to be monitored.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter		Rating	Unit
V_{CC}	Supply Voltage		-0.3 to 6.0	V
	All other Inputs		-0.3 to Vcc+0.3	V
I_{IN}	Input Current (Vcc, /MR)		20	mA
	Output Current (RESET, /RESET)		20	mA
P_D	Power Dissipation, @ T_A = 25℃ SOT23-5		0.4	W
P_D	Power Dissipation, @ T_A = 25℃ SOT143-4		0.32	W
	Operating Temperature		-40 to 125	°C
	Junction Temperature		150	°C
	Storage Temperature		-65 to 150	°C
	Lead Temperature (soldering, 10s)		260	°C
ESD	HBM, JEDEC:JESD22-A114	I/O to GND	4	kV
		Others	8	

DC Electrical Characteristics

(V_{CC} Typ=5V for L/M/J Models, 3.3V for T/S Models, 3V for R Models, 2.5V for Z Models); unless otherwise noted.

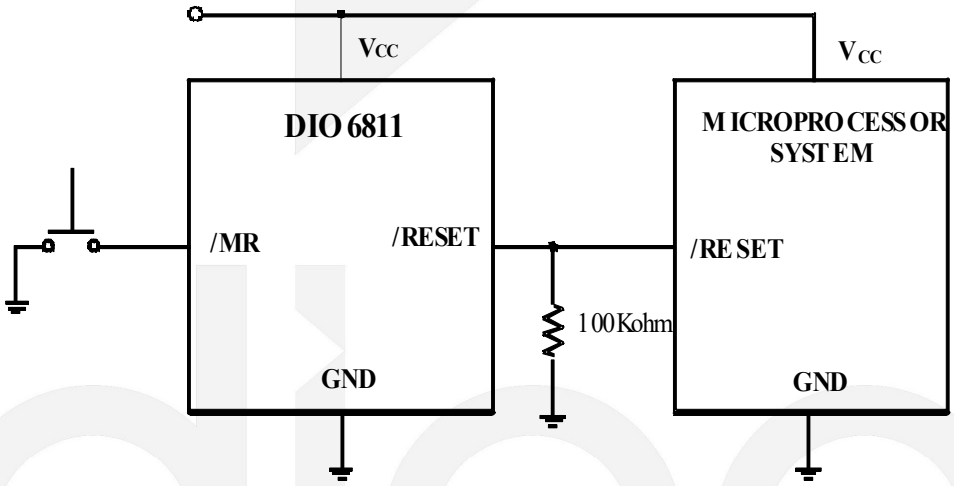
Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage		T_A = 0°C to 70°C	1.0		5.5	V
Supply current	I_{VCC}	Vcc=2.0V		8		uA
		Vcc=3.0V		10		
		Vcc=5.0V		14		
Reset Threshold	V_{RES}	DIO681_L	4.537	4.63	4.723	V
		DIO681_M	4.292	4.38	4.468	
		DIO681_J	3.92	4.00	4.08	
		DIO681_T	3.003	3.08	3.157	
		DIO681_S	2.85	2.93	3.00	
		DIO681_R	2.564	2.63	2.696	
		DIO681_Z	2.262	2.32	2.378	
Temperature coefficient of reset threshold	T_C			21		ppm/°C
VCC to RESET(/RESET) Delay		V_{CC} = V_{TH} to (V_{TH} –100mV)		23		μs
Reset Active Timeout Period		T_A = - 40°C to 125°C	160	240	560	ms
MANUAL RESET						
Minimum Pulse width			10			μs
Glitch Immunity				100		ns
RESET (/RESET) Propagation Delay				0.5		μs
Pull-Up Resistance				4		MΩ
The Manual Reset Circuit Will Act On:						
An Input Rising Above		V_{CC} > $V_{TH(MAX)}$, DIO681_L/M/J	2.3			V
An Input Falling Below		V_{CC} > $V_{TH(MAX)}$, DIO681_L/M/J			0.8	V
An Input Rising Above		V_{CC} > $V_{TH(MAX)}$, DIO681_R/S/T/Z	0.7×V_{CC}			V
An Input Falling Below		V_{CC} > $V_{TH(MAX)}$, DIO681_R/S/T/Z			0.25×V_{CC}	V

Electrical Characteristics (Continued)

(V_{CC} Typ=5V for L/M/J Models, 3.3V for T/S Models, 3V for R Models, 2.5V for Z Models); unless otherwise noted.

RESET (/ RESET) OUTPUT VOLTAGE						
Low (DIO6811R/S/T/Z)		V_{CC} = $V_{TH(MIN)}$, I_{SINK} = 1.2mA			0.3	V
Low (DIO6811L/M/J)		V_{CC} = $V_{TH(MIN)}$, I_{SINK} = 3.2mA			0.4	V
Low (DIO6811R/S/T/Z/L/M/J)		V_{CC} > 1.0 V, I_{SINK} = 50μA			0.3	V
High (DIO6811R/S/T/Z)		V_{CC} > $V_{TH(MAX)}$, I_{SOURCE} = 500μA	0.8×V_{CC}			V
High (DIO6811L/M/J)		V_{CC} > $V_{TH(MAX)}$, I_{SOURCE} = 800μA	V_{CC}– 1.5			V
Low (DIO6812R/S/T/Z)		V_{CC} = $V_{TH(MAX)}$, I_{SINK} = 1.2mA			0.3	V
Low (DIO6812L/M/J)		V_{CC} = $V_{TH(MAX)}$, I_{SINK} = 3.2mA			0.4	V
High (DIO6812R/S/T/Z/L/M/J)		1.8V<V_{CC}<$V_{TH(MIN)}$, I_{SOURCE}= 150μA	0.8×V_{CC}			V
Specifications subject to change without notice.						

Typical Application



Applications Information

MANUAL RESET

The DIO6811/6812 is equipped with a manual reset input. This input is designed to operate in a noisy environment where unwanted glitches could be induced. These glitches could be produced by the bouncing action of a switch contact, or where a manual reset switch may be located some distance away from the circuit (the cabling of which may pick-up noise).

The manual reset input is guaranteed to ignore logically valid inputs that are faster than 100ns and to accept inputs longer in duration than 10μs.

BENEFITS OF A VERY ACCURATE RESET THRESHOLD

Because the DIO6811/6812 can operate effectively even when there are large degradations of the supply voltages, the possibility of a malfunction during a power failure is greatly reduced. Another advantage of the DIO6811/6812 is its very accurate internal voltage reference circuit. Combined, these benefits produce an exceptionally reliable microprocessor supervisory circuit.

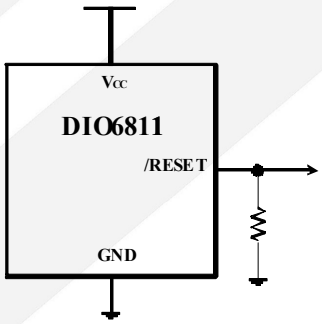


Figure 1 Ensuring a Valid /RESET Output Down to VCC = 0V

ENSURING A VALID RESET OUTPUT DOWN TO VCC = 0V

When VCC falls below 1.0V, the DIO6811/6812's /RESET no longer sinks current. Therefore, a high impedance CMOS logic input connected to /RESET may drift to undetermined logic levels. To eliminate this problem, a 100kΩ resistor should be connected from /RESET to ground.

RESET OUTPUT

On power-up and after VCC rises above the reset threshold, an internal timer holds the reset output active for 240ms (typical). This is intended as a power-on reset signal for the processor. It allows time for both the power supply and the microprocessor to stabilize after power-up. If a power supply brownout or interruption occurs, the reset output is similarly activated and remains active for 240ms (typical) after the supply recovers. This allows time for the power supply and microprocessor to stabilize.

The DIO6811 provides an active low reset output (/RESET) while the DIO6812 provides an active high output (/RESET). During power-down of the DIO6811, the /RESET output remains valid (low) with VCC as low as 1V. This ensures that the microprocessor is held in a stable shutdown condition as the supply falls and also ensures

that no spurious activity can occur via the microprocessor as it powers up.

Glitch Immunity

The DIO6811/6812 contains internal filtering circuitry providing glitch immunity from fast transient glitches on the power supply line.

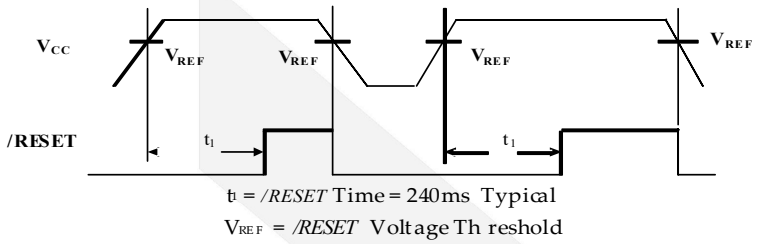


Figure 2 Power Fail /RESET Timing

INTERFACING TO OTHER DEVICES Output

The DIO6811/6812 is designed to integrate with as many devices as possible. One feature of the DIO6811/6812 is the reset output, which is directly proportional to VCC (this is guaranteed only while VCC is greater than 1V). This enables the part to be used with both 3V and 5V, or any nominal voltage within the minimum and maximum specifications for VCC.

CONTACT US

Dioo is a professional design and sales corporation for high-quality and performance analog semiconductors. The company focuses on industry markets, such as, cell phone, handheld products, laptop, and medical equipments and so on. Dioo's product families include analog signal processing and amplifying, LED drivers and charger IC. Go to http://www.dioo.com for a complete list of Dioo product families.

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