DIO6833E
High Efficiency, 2A, Two-Cell Boost Li-Ion Battery Charger Preliminary Specification

Features

- Low Profile QFN3x3 Package for Portable Applications
- Integrated Synchronous Boost with 18V Rating Low RDSON FETs for High Charge Efficiency
- Charge Voltage Accuracy: ±0.5%
- Trickle Current / Constant Current / Constant Voltage Charge Mode
- Adaptive Input Current Limit with selectable threshold
- Maximum 2A Constant Charge Current
- Charge Current Information Indication.
- Programmable Charge Timeout
- Programmable Constant Charge Current
- Constant Voltage Selectable
- Thermal Regulation Protection
- External Shutdown Function
- Input Voltage UVLO and OVP
- Over Temperature Protection
- Output Short Circuit Protection
- Charge Status Indication
- Normal Synchronous Boost Operation When Battery Removed

Descriptions

DIO6833E is a 3.6-5.5V, 2A two-cell synchronous boost Li-Ion battery charger integrates 1MHz switching frequency and full protection functions. The charge current up to 2A can be programmed by using the external resistor for different portable applications and indicates the charger current information simultaneous. It also has a programmable charge timeout and adaptive input current limit with selectable threshold for safety battery charge operation. DIO6833E can disconnect output when there is output short circuit or shutdown happens. It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

DIO6833E along with small QFN3x3 footprint provides small PCB area application.

Applications

- Cellular Telephones, PDA, MP3 Players, MP4 Players
- Digital Cameras
- Bluetooth Applications
- PSP Game Players, NDS Game Players
- Notebook

Ordering Information

Order Part Number	Top Marking		T_A	Package	
DIO6833ECL16	DIO3E	Green	-40 to 85°C	QFN3*3-16	Tape & Reel, 5000

Pin Assignments

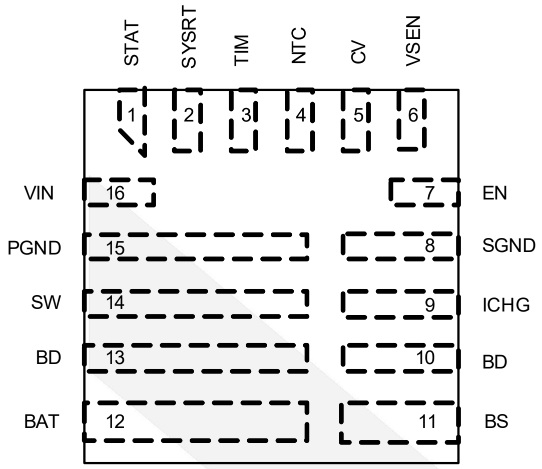


Figure 1 Pin Assignment (Top View)

Pin Definitions

Pin name	Description
SW	Switch node pin. Connect to external inductor.
STAT	Charge status indication pin. It is open drain output pin and pull high to VIN thru a LED to indicate the charge in process. When the charge is off done, LED is off.
VIN	Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area.
CV	Battery CV voltage selection pin. Pull down for 8.4V cell voltage and pull up for 8.7V cell voltage.
VSEN	Voltage sense of VIN. If the voltage drops to internal 1.195V reference voltage, the VIN will be clamped to setting value and input current will be limited.
TIM	Charge time limit pin. Connect this pin with a capacitor to ground. Internal current source charge the capacitor for charge time limit. TC charge time limit is about 1/10 of CC charge time.
ICHG	Charge current program pin, pull down to GND with a resistor R_{ICHG}. The mirror current about 1/10800 of the blocking FET current will dump into the external resistor thru ICHG pin and compared to the internal reverence 1V. So I_{CC}=(1V/ R_{ICHG})x10800, R_{ICHG}≤42kΩ.
NTC	Thermal protection pin. UTP threshold is typical 75%VSVIN and OTP threshold is typical 30% VSVIN. Pull up to SVIN can disable charge logic and make the IC operate as normal boost regulator. Pull down to ground can shut down the IC.
BAT	Battery positive pin.
BS	Boost-Strap pin. Supply Rectified FET's gate driver. Decouple this pin to SW with 0.1μF ceramic cap.
BD	Connect to the Drain of internal Blocking FET. Bypass at least 4.7μF ceramic cap to GND.
EN	Enable control pin. High logic for enable on, and low logic for enable off.
SYSRT	System ON/OFF control pin. When VBAT is lower than 6V, SYSRT pin outputs low logic to turn off the system operation; when VBAT is high than 6V, SYSRT pin outputs high logic to turn on the system operation.
SGND	Signal ground pin.
PGND	Power ground pin.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Rating	Unit
VIN, BAT, SW, NTC, STAT, BD, EN, ICHG, CV, VSEN	18	V
TIM, SYSRT	6	V
BS-SW Voltage	6	V
SW Pin current continuous	5	A
Junction Temperature Range	-40 to 125	°C
Lead Temperature	260	°C
Storage Temperature Range	-60 to 150	°C

Recommend Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended Operating conditions are specified to ensure optimal performance to the datasheet specifications. DIOO does not Recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter	Rating	Unit
VIN	3.6 to 5.5	V
BAT, SW, NTC, STAT, BD, EN, ICHG, CV, VSEN	-0.3 to 16	V
TIM, SYSRT	-0.3 to 5.5	V
SW Pin current continuous	5	A
Junction Temperature Range	-40 to 125	°C
Ambient Temperature Range	-40 to 85	°C

Electrical Characteristics

V_S=5V, V_{CM}=V_{OUT}=2.5V, R_L=2kΩ, C_L=100pF, T_A=25°C, unless otherwise specified.

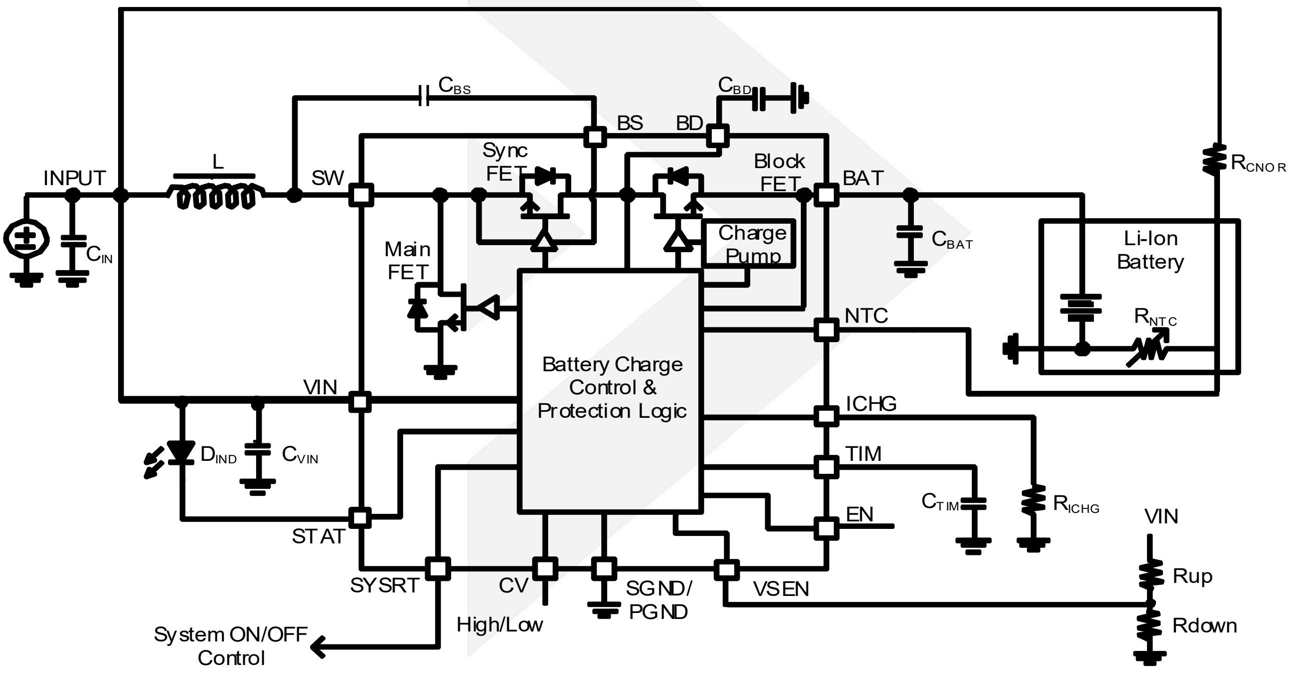
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Bias Supply (VIN)						
V_{IN}	Supply voltage		3.6		16	V
V_{UVLO}	V_{IN} under voltage lockout threshold	V_{IN} rising and measured from V_{IN} to GND		2.8		V
ΔV_{UVLO}	V_{IN} under voltage lockout hysteresis	Measured from V_{IN} to GND		100		mV
V_{OVP}	Input overvoltage protection	V_{IN} rising and measured from V_{IN} to GND	6			V
ΔV_{OVP}	Input overvoltage protection hysteresis	Measured from V_{IN} to GND		0.5		V
Quiescent Current						
I_{BAT}	Battery discharge current	Shutdown IC		7		μA
I_{IN}	Input quiescent current	Disable Charge		0.2		mA
Oscillator and PWM(TBD)						
f_{SW}	Switching frequency			1000		kHz
T_{MINOFF}	Main N-FET minimum off time	With 16V rating		100		ns
T_{MAXOFF}	Main N-FET maximum off time	With 16V rating		30		μs
T_{MINON}	Main N-FET minimum on time	With 16V rating		100		ns
Power MOSFET						
R_{NFET_M}	$R_{DS(ON)}$ of Main N-FET			50		mΩ
R_{NFET_R}	$R_{DS(ON)}$ of Rectified N-FET			35		mΩ
R_{NFET_B}	$R_{DS(ON)}$ of Blocking N-FET			35		mΩ
Voltage Regulation						
V_{CV}	2-Cell CV charge mode voltage	V_{CV}<1V	8.358	8.40	8.442	V
		V_{CV}>2V	8.656	8.70	8.743	
V_{CV}	High level logic for CV		2			V
V_{CV}	Low level logic for CV				1	V
ΔV_{RCH}	2-Cell Recharge Voltage			200		mV
V_{TRK}	2-cell TC charge mode battery voltage threshold	V_{BAT} rising edge threshold	5.4	5.6	5.8	V
Charge Current						

	Internal charge current accuracy for Constant Current Mode	I_{CC}=1080mA	-10%		10%	
I_{TERM}	Termination current	I_{CC}=1080mA		108		mA
Output Voltage OVP						
V_{OVP}	Output voltage OVP threshold		105%	110%	115%	V_{CV}
Input Voltage Threshold for Adaptive Current Limit						
$V_{Threshold}$	Voltage reference of VSEN		1.171	1.195	1.219	V
Timer						
T_{TC}	V_{BAT}<V_{TRK} timeout	C_{TIM}=330nF	0.425	0.5	0.575	hour
T_{STOP}	Charge termination timeout	C_{TIM}=330nF	3.825	4.5	5.175	hour
T_{MC}	Charge mode change delay time			30		ms
T_{TERM}	Termination delay time			30		ms
T_{RCHG}	Recharge time delay			30		ms
System ON/OFF Control						
V_{HSYSRT}	High logic of system ON/OFF control		2.1			V
V_{LSYSRT}	Low logic of system ON/OFF control				0.6	V
V_{HYSSYS}	Hysteresis for positive and negative edge			100		mV
Linear charger Mode						
I_{LCHG}	Battery Charger current when the blocking FET is in linear mode	V_{BAT}<V_{TRK}		25%		I_{CC}
I_{LPEAK}	Peak linear current when Battery is absent			1		A
V_{BD}	Bus voltage regulation		5.8	6	6.2	V
Enable ON/OFF Control						
V_{ENH}	High level logic for enable control		1.5			V
V_{ENL}	Low level logic for enable control				0.4	V
Battery Thermal Protection NTC						
OTP	Over temperature detection voltage threshold	Battery temperature rise		30%		V_{VIN}
OTP	Over temperature detection voltage hysteresis	Battery temperature drop		2%		V_{VIN}
UTP	Under temperature detection voltage threshold	Battery temperature drop		75%		V_{VIN}
UTP	Under temperature detection voltage hysteresis	Battery temperature rise		5%		V_{VIN}

Thermal Regulation And Thermal shutdown						
T_{REG}	Thermal regulation threshold			120		°C
T_{SD}	Thermal shutdown temperature	Rising Threshold		160		°C
T_{SDHYS}	Thermal shutdown temperature hysteresis			30		°C

Specifications subject to change without notice.

Typical Applications



General Function Description Operation

DIO6833E is a 3.6-5.5V, 2A two-cell synchronous boost Li-Ion battery charger integrates 1MHz switching frequency and full protection functions. The charge current up to 2A can be programmed by using the external resistor for different portable applications and indicates the charger current information simultaneous. It also has a programmable charge timeout and adaptive input current limit for safety battery charge operation. DIO6833E can disconnect output when there is output short circuit or shutdown happens. It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

Charging Status Indication Description

1. Charge-In-Process – Pull and keep STAT pin to Low;
2. Charge Done-Pull and keep STAT pin to High;
3. Fault Mode (UVLO, TSD, NTC error, timeout, BAT OVP)-Output high and low voltage alternatively with 1.3Hz frequency. Connect a LED from VIN to STAT pin, LED ON means Charge-in-Process, LED OFF means Charge Done, LED Flashing with 1.3Hz means Fault Mode.

Switching Mode Boost Charger Basic Operation Description

Switching Mode Control Strategy

DIO6833E is a switching mode Boost charger for the applications with USB power input. DIO6833E utilizes quasi-fixed frequency constant OFF time control to simplify the internal close-loop compensation design. Slope compensation is not necessary for the stable operation. The quasi-fixed frequency settled at 1MHz is easy for the size minimization of peripheral circuit design. During the light load operation, when the output voltage of the internal error amplifier VC is lower than the minimum threshold 0.3V, the OFF time is going to be stretched to achieve frequency fold back.

Operation Principle

DIO6833E can normally work with or without Li-Ion battery both.

Battery Present

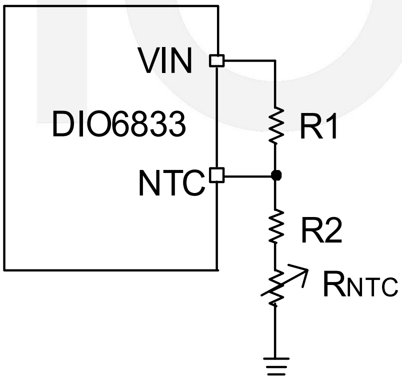
Before DIO6833E start-up, C_{BD} is charged by the battery thru the body diode of blocking FET, and V_{BD} equals to V_{BAT}.

If the plug in input voltage V_{IN} is higher than V_{BD}=V_{BAT}, C_{BD} is charged by V_{IN} further thru the body diode of sync-FET. Under this condition, the Boost charger operates in light load mode and regulates the V_{BD} at 6V and the blocking FET works in linear charge mode. Note that, charging current would not be increased to I_{CC} when the block FET operates in linear mode. With the increasing of V_{BAT}, when V_{BAT} is higher than both V_{IN} and V_{TRK} the blocking FET is fully turned on and the switching mode boost charger takes over the battery charging. The current in the blocking FET is mirrored to be as the charging current I_{CHG}. If V_{IN} is lower than V_{BD}=V_{BAT} at the plug in time, the switching mode boost charger starts work directly.

During the charging mode, constant (trickle) charging current loop is active first. When V_{BAT} equals to constant voltage threshold V_{CV}, constant voltage loop takes over and pull down the charging current. When I_{CHG} is lower than the termination current threshold I_{TERM}, the main FET of boost charger is turned off firstly. Sync-FET and blocking FETs are turned off together when the current is down to zero. Then, DIO6833E is waiting for recharge mode.

NTC Resistor

DIO6833E monitors battery temperature by measuring the input voltage and NTC voltage. The controller triggers the UTP or OTP when the rate K (K= V_{NTC}/V_{VIN}) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.
Choose R_1 and R_2 to program the proper UTP and OTP points.



The calculation steps are:

1. Define K_{UT}, K_{UT}=70~80%
2. Define K_{OT}, K_{OT}=28~32%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at U_{TP} threshold and R_{OT} at OTP threshold.
4. Calculate R_2

$$R_2 = \frac{K_{OT}(1-K_{UT})R_{UT} - K_{UT}(1-K_{OT})R_{OT}}{K_{UT} - K_{OT}}$$

5. Calculate R_1

$$R_1 = (1/K_{OT} - 1)(R_2 + R_{OT})$$

If choose the typical values K_{UT}=75% and K_{OT}=30%, then

$$R_2 = 0.17R_{UT} - 1.17R_{OT}$$

$$R_1 = 2.3(R_2 + R_{OT})$$

Thermal Regulation and Protection

When the IC's junction temperature reaches T_{REG} (about 120°C), the charger reduces its output current to prevent overheating. If the temperature increases beyond T_{SD}; charging is suspended, and STAT is pulsed. Charging resumes after the die cools to about 120°C.

Battery Absent

If there's no battery connection detected thru NTC pin, DIO6833E operates as a normal switching mode boost converter and pulses STAT pin. When V_{IN} is higher than UVLO threshold, the blocking FET is softly turned on. After the blocking FET fully turn-on, switching mode boost converter starts work. The internal current loop and voltage loop are active both.

Basic Protection Principle

DIO6833E has fully battery charging protection. When the input over voltage protection, the output over voltage protection, the thermal protection or the timeout protection happens, the main FET of the boost charger is turned off immediately. The sync-FET and the blocking FET are turned off later when the current is down to zero. When the V_{BAT} is lower than V_{TRK}.

Adaptive Input Current Limit Principle

DIO6833E has adaptive input current limit function.. The high charging current will caused a voltage drop at V_{IN} when the input DC source is over load. When VSEN drops below the internal 1.195V reference, DIO6833E will decrease the duty cycle to reduce the charging current until input voltage recovers back.

Constant Voltage Threshold Program Principle

DIO6833E can program the constant voltage threshold thru the CV pin. When V_{CV} is higher than 2V, the constant voltage threshold is 8.7V; when V_{CV} is lower than 1V, the constant voltage threshold is 8.4V.

Applications Information

Because of the high integration of DIO6833E, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L, and timer capacitor C_{TIM} need to be selected for the targeted applications specifications.

Timer capacitor C_{TIM}

The charger also provides a programmable charge timer. The charge time is programmed by the capacitor connected between the TIM pin and GND. The capacitance is given by the formula:

$$C_{TIM} = 2*10^{-11} T_{STOP} \qquad \text{Unit:F}$$

T_{STOP} is the target charge time, unit: s.

Input capacitor C_{IN}

The ripple current through input capacitor is greater than

$$I_{CIN\_RMS} = \frac{V_{IN}*(V_{OUT} - V_{IN})}{2\sqrt{3}*L*F_{SW}*V_{OUT}}$$

X5R or X7R ceramic capacitors with greater than 4.7μF capacitance are recommended to handle this ripple current.

Output capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. This ripple voltage is related to the capacitance and its equivalent series resistance (ESR). For the best performance, it is recommended to use X5R or better grade low ESR ceramic capacitor. The voltage rating of the output capacitor should be higher than the maximum output voltage. The minimum required capacitance can be calculated as:

$$C_{OUT} = \frac{I_{CC}*(V_{OUT} - V_{IN})}{F_{SW} \times V_{OUT} \times V_{RIPPLE}}$$

V_{RIPPLE} is the peak to peak output ripple; I_{CC} is the setting charge current.

For DIO6833E, output capacitor is paralleled by C_{BD} and C_{BAT}, for smaller output ripple noise, each capacitor with greater than 10μF capacitance is recommended.

Inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{I_{CC} \times F_{SW} \times 40\%}$$

Where FSW is the switching frequency and I_{CC} is the setting charge current.

The DIO6833E is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{CC} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve a good overall efficiency.

Layout Design

The layout design of DIO6833E regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{VIN}, L, and C_{BD}.

1) The loop of main MOSFET, rectifier diode, and C_{BD} must be as short as possible.

2) It is desirable to maximize the PCB copper area connecting GND pin to achieve the best thermal and noise performance.

3) C_{VIN} must be close to pin VIN and GND.

4) The PCB copper area associated with SW pin must be minimized to avoid the potential noise problem.

5) The small signal component R_{ICHG} must be placed close to IC and must not be adjacent to the SW net on the PCB layout to avoid the noise problem.

CONTACT US

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